

## **REMARKS**

Claims 1-20 are pending in the application. Claims 1-8, 10, 16, 19, and 20 stand rejected. Applicants gratefully acknowledge the Examiner's indication that claims 9, 11-15, 17 and 18 include allowable subject matter and would be allowable if rewritten as indicated. The Examiner's reconsideration of the claim rejections is respectfully requested in view of the following remarks.

### **Claim Rejections - § 103**

(1) Claims 1-3, 5, 10, 16 and 19-20 are rejected as being unpatentable over Applicant's admitted prior art FIG. 1 (hereafter, "APA") in view of U.S. Patent Application Publication 2003/0142773 to Shirota. It is respectfully submitted that at the very least, claims 1, 16, and 20 are patentable over the combination of APA and Shirota.

It is submitted that the combination of APA and Shirota does not disclose or suggest *a clock signal generating circuit that generates at least two clock signal groups, comprising first and second clock signal groups wherein each of the first and second clock signal groups are composed of clock signals having different phases; and a data recovery circuit that recovers effective data from serial data by oversampling the serial data by using a dynamically selected one of at least two clock signal groups, as essentially claimed in claim 1.*

In pages 2-3 of the Final Action, the Examiner erroneously interprets individual clock signals CLKA, CLKB, and CLKC, generated by PLL 11 of the APA, as being first, second, and third clock signal groups. The Examiner is essentially interpreting a clock signal group as including only one clock signal. However, this interpretation contradicts the claim language of claim 1. A clock signal group is recited in claim 1, as being

*composed of clock signals*, and not a single clock signal. Even assuming, *arguendo*, that a clock signal group were only comprised of a single clock signal, APA is still deficient. For example, the oversampler 12 of APA would then be performing oversampling using three clock signal groups, which is different from the claimed data recovery circuit which performs oversampling using a dynamically selected one of at least two clock signal groups. The Examiner's reliance on Shirota to cure the deficiencies of APA in this regard is respectfully misplaced.

The Examiner contends that Shirota discloses dynamically selecting one of at least two clock signal groups. In support of this contention, the Examiner cites figures 1 and 2 of Shirota and paragraph 35 of Shirota which states that the "DCR circuit 104 selects from the clock signal group 109 the optimum clock signal for loading the receive output". However, the cited figures and statement actually contradict the Examiner's contention. For example, figures 1 and 2 merely illustrate a single clock signal group 109 and the cited statement merely discloses selecting a single clock signal from a single clock signal group 109, which is not the same as dynamically selecting one of at least two clock signal groups.

Indeed, Shirota's teachings of a DCR circuit 104 that selects from a single clock signal group is not relevant and teaches nothing more than what is disclosed by the APA. The Examiner can neither fairly nor legally establish obviousness by combining the teachings of the single clock signal group of APA with the single clock signal group 109 of Shirota and contend that it would have been obvious to implement the invention of claim 1 which essentially implements two or more clock signals groups and dynamically selects between the groups for data recovery.

It is further submitted that the combination of APA and Shirota does not disclose or suggest the selection of a clock signal group depending upon the number of edges of clock signals being within an eye open region of the serial data, as essentially claimed in claim 1. The Examiner seemingly relies on Shirota as disclosing this limitation, but offers no explanation.

For at least these reasons, the Final Action fails to present a *prima facie* case of obviousness against claim 1. For similar reasons, claims 16 is not obvious in view of the combination of APA and Shirota as such a combination clearly does not disclose or suggest, e.g., a data recovery circuit that recovers the effective data from the serial data by sampling the serial data by the sampling clock signals of a dynamically selected one of the at least two sampling clock signal groups, as recited in claim 16.

Furthermore, for similar reasons discussed above, the combination of APA and Shirota does not teach or suggest, e.g., a first and second set of OSR sampling clock signals, wherein all the 2 x OSR sampling clock signals have different phases; and wherein the selected set of OSR sampling clock signals has been dynamically selected so as to sample the serial data by a plurality of sampling clock signals having edges within the eye open region of the serial data, as recited in claim 20.

Accordingly, claims 1, 16, and 20 are not obvious in view of APA and Shirota. Moreover, claims 2-3, 5, 10, and 19 are not obvious in view of APA and Shirota at least by virtue of their dependence from respective base claims 1 or 16.

The following obviousness rejections are also asserted:

(2) Claims 4 and 6 are rejected as being unpatentable over APA, Shorota, and U.S. Patent 6,807,233 to Sato.

(3) Claim 7 is rejected as being unpatentable over APA, Shirota and U.S. Patent 5,528,198 to Baba.

(4) Claim 8 is rejected as being unpatentable over APA, Shirota and U.S. Patent 7,103,343 to Boss.

The above obviousness rejections (2~4) are legally deficient as a matter of law at least to the extent that the rejections are premised on the combination of APA and Shirota, at least for the reasons stated above for the base claim 1, from which claims 4, 6, 7, and 8 depend.

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

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